Amendments to the Specification:

Please replace the paragraph beginning at page 13, line 14, with the following rewritten paragraph:

In the illustrated embodiment, the automated detection circuitry in control circuit 28 is implemented using one or more OR gates that together implement a logical-OR operation, as represented at block 50. In the illustrated implementation, each of the bits in each of the communication registers 46 is fed to logic gate 50 to perform logical-OR operation on all of the bits in all of the communication registers. Thus, for example, in the implementation illustrated in Fig. 4, assuming N communication registers, each being W bits in width, a W x N bit binary OR gate may be utilized to generate the interrupt signal. In the illustrated embodiment, for example, four network ports and dedicated 64-bit communication registers may be used, whereby block ~~bock~~ 50 may incorporate 256 binary inputs.